# P-11: Electrical Properties and Stability of Dual-Gate Coplanar Homojunction Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistor

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## Abstract

*The electrical characteristics and stabilities of dual-gate (DG) coplanar homojunction amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) are described. When the gate voltage is applied on top and bottom electrodes, the DG a-IGZO TFT showed an excellent electrical performance with the sub-threshold swing of 99 mV/dec, the mobility of 15.1 $cm^2/V{\cdot}s$ and the on-off ratio of $10^9$. Under positive bias temperature stress, the device threshold voltage shifts about +4.5V after 10,000 seconds, while its shifts under negative bias temperature stress are very small. The effect of TFT illumination is also discussed.*

## 1. Introduction

It is well known that the metal-oxide-semiconductor field effect transistors can have a better electrical performance when a larger portion of channel area is controlled by an additional gate electrode. [1] The dual-gate or double-gate (DG) structure has already been proposed for a sub-micron silicon complimentary metal-oxide-semiconductor (CMOS). The DG amorphous silicon (a-Si:H) TFTs have also been investigated to provide an effective light shielding that guarantee the TFT's electrical reliability under illumination. [2, 3] However, the presence of bias on the additional gate electrode introduces unwanted shifts in a-Si:H TFT sub-threshold swing (SS) and threshold voltage. To address this problem, the additional gate electrode has been grounded to provide reliable circuit operation in a pixel array. [3, 4]We believe that the dual-gate a-IGZO TFT structure has the advantage of producing an enhanced device performance and stability under light illumination.

It was previously reported that the coplanar homojunction a-IGZO TFT has a good ohmic source/drain (S/D) junction and is capable of achieving small channel lengths. [5, 6] In this paper, we describe the DG coplanar homojunction a-IGZO TFT electrical characteristics, and stability under bias temperature stress (BTS) and under illumination.

## 2. Experimental

### 2.1. a-IGZO TFT structure

Figure 1 shows processing step during the DG TFT fabrication. [5] To form a bottom gate electrode, a 100 nm-thick Mo film was deposited by a direct-current sputtering on glass substrate (Corning 1737) and patterned to form the bottom gate electrode ***(a)***. A 200 nm-thick SiOx layer was deposited by plasma enhanced chemical vapor deposition (PECVD) at 340 °C which will be used as a bottom gate insulator ***(b)***. The a-IGZO film (30 nm) was D.C. sputtered at room temperature and defined using a diluted hydrochloric acid ***(c)***. A 150 nm a-$SiO_X$ channel protection layer (CPL) was sputtered and patterned by dry etching ***(d)***. The CPL defines the TFT width (W) and length (L). The CPL

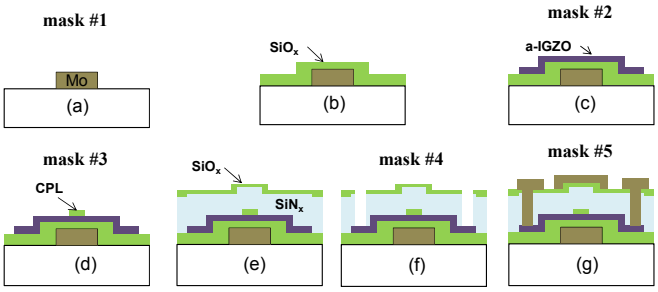
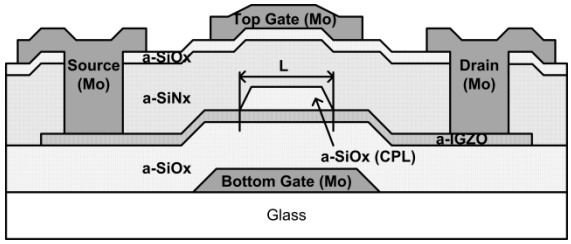



**Figure 1 A schematic representation of the processing steps used during the DG TFT fabrication.**

patterning was followed by a PECVD at 250 °C of bi-layer passivation of 300 nm-thick amorphous silicon nitride (a-$SiN_X$:H) and 50 nm-thick a-$SiO_X$. During the a-$SiN_X$:H PECVD process, hydrogen in the reactive PECVD chamber and/or in the a-$SiN_X$:H layer dopes the exposed a-IGZO region and increases its electrical conductivity ***(e)***. Next the contact vias were formed in top passivation bi-layer by dry etching ***(f)***, followed by the sputtering and patterning of 100 nm-thick Mo source/drain electrodes. At the same time the Mo top gate is formed ***(g)***. It should be noticed that in such device structure Mo metal gate and source/drain contacts do not overlap; although there is some overlap between Mo metal gate and the hydrogen doped S/D contact regions. There is sepera-



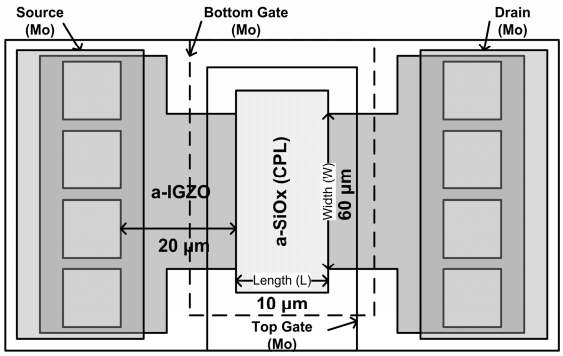




**Figure 2. (Top) Schematic cross-section and (Bottom) top view of the fabricated DG coplanar homojunction a-IGZO TFT.**

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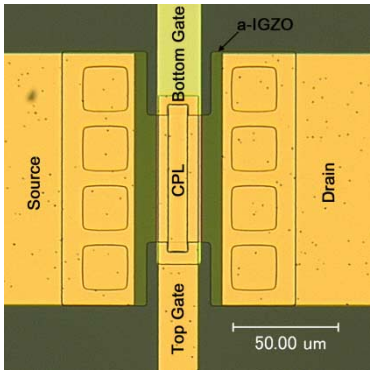


**Figure 3. The microscopic image of the fabricated DG coplanar homojunction a-IGZO TFT.**

-tion of about 20 μm between CPL edge and S/D via edge. Finally the TFT underwent a thermal annealing process at 270 ºC in atmosphere. Figure 2 shows schematic cross-section and top view of the DG TFT. The macroscopic image of the DG TFT is shown in Figure 3.

## 2.2. Electrical measurements

All the TFTs' electrical transfer characteristics were measured using an Agilent 4156C parameter analyzer with the source acting as the ground and a gate-to-source voltage ($V_{GS}$) is applied and swept on both top and bottom gate electrodes at the same time; $V_{ST} = V_{BG} = V_{TG}$. During transfer characteristics measurement, the $V_{GS}$ is sweeping from -10 to 15 V and from 15 to -10 V at 0.2 V intervals. The reverse direction sweeping of $V_{GS}$ is used to check for device hysteresis.

For bias-temperature stress (BTS) experiments, a stress voltages, $V_{ST}$ = +15 V or -15V are used for positive BTS (PBTS) and negative BTS (NBTS), respectively. The drain terminal is shorted to source terminal. The stress voltage is also applied on top and bottom gates. The stress temperature is fixed at 80 °C.

To check the device characteristics under illumination, we expose DG TFTs to Mercury-Xeon (Oriel 6291) arc lamp through a microscope via a fiber optic (with 10mW/cm$^2$ of illumination over the top surface of the device). The wavelength (λ) of the illuminated light has the spectral range from 200 to 2,400 nm.

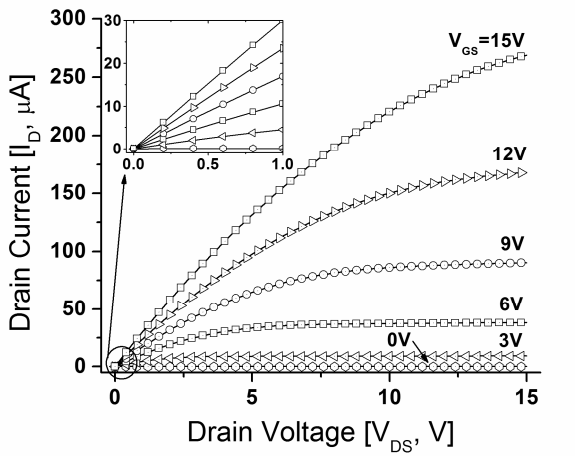


**Figure 4. Output characteristics of DG coplanar homojunction a-IGZO TFT where top and bottom gates are synchronized, (inset) details for 0 V ≤ $V_{DS}$ ≤ 1 V.**

# 3. Results and Discussion

## 3.1. Device Electrical Parameters Extraction

Figure 4 shows the output characteristics of the DG a-IGZO TFT. The inset of Figure 4 shows details of output characteristics for the drain voltage ($V_{DS}$), 0 V ≤ $V_{DS}$ ≤ 1 V; no current crowding is found near the origin. Therefore, it can be concluded that the Mo/a-IGZO contact is ohmic in nature in such device configurations. [7]

The TFT transfer characteristic is also measured. Figure 5 illustrates the linear ($V_{DS}$ = 0.1 V) and saturation ($V_{DS}$ = 15 V) regime transfer characteristics. The W and L of the a-IGZO TFT is 60 μm and 10 μm, respectively. We extract device parameters, such as $\mu_{EFF}$ and threshold voltage ($V_{TH}$) based on the standard MOSFET drain current ($I_D$) equation: in the linear regime of the operation,

$$I_D = \mu_{EFF} C_{DI} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \qquad (1)$$

and in the saturation regime of the operation. [8]

$$I_D{}^{1/2} = \left\{ \frac{\mu_{EFF} C_{DI}}{2} \frac{W}{L} \right\}^{1/2} (V_{GS} - V_{TH}) \qquad (2)$$

where W and L are the channel width and length of the TFT, respectively. The $V_{GS}$ is gate voltage and $C_{DI}$ is gate insulator capacitance per unit area; $C_{DI}$=$C_{TI}$+$C_{BI}$ where $C_{TI}$ and $C_{BI}$ are the capacitance per unit area for top and bottom gate insulators, respectively. The dielectric constant for a-SiOx and a-SiNx is 3·$\varepsilon_0$ and 7·$\varepsilon_0$, respectively. The best linear fit to equation (1) and (2) between 90% and 10% of the maximum $I_D$ is used for the $V_{TH}$ and $\mu_{EFF}$ extraction. The sub-threshold swing (SS) is extracted from the sub-threshold region data.

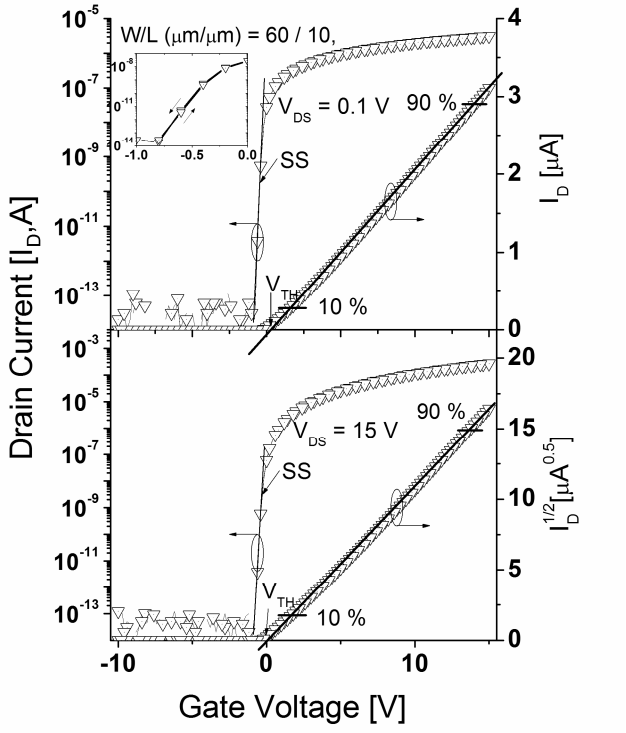


**Figure 5. Transfer characteristic of DG a-IGZO TFT in (Top) linear regime; $V_{DS}$ = 0.1 V and (Bottom) saturation regime; $V_{DS}$ = 15 V.**

$$SS = \left(\frac{\partial log(I_D)}{\partial V_{GS}}\right)^{-1} \quad (3)$$

The drain current range one order below to one order above from a maximum ($\partial \log I_{DS}/\partial V_{GS}$) point is used to calculate the SS. More details about device parameter extraction can be found in [9]. The extracted device parameters in linear and saturation regime are summarized in Table 1.

### 3.2. a-IGZO TFT Electrical Characteristics

Our DG a-IGZO TFT has following room temperature properties: $\mu_{EFF}$ = 15.07 $cm^2/V{\cdot}s$, $V_{TH}$ = 0.37 V, SS = 99 mV/dec, off-state drain current ($I_{OFF}$) ~ $10^{-13}$A and on-off current ratio over $10^9$. These results indicate a very good electrical performance of the DG a-IGZO TFT. By comparing with the typical a-IGZO coplanar homojunction TFTs which have been previously reported [5, 6], the considerable improvements in $I_{ON}$ and SS with DG TFT structure are noteworthy.

In Table 1, we have compared these results with those obtained for DG a-IGZO TFT with bottom gate (BG) bias condition. For BG bias condition, the $V_{GS}$ is applied only on bottom gate while the top gate is grounded. The BG TFT structure is similar to a traditional TFT structure. In DG a-IGZO TFT, since the $V_{GS}$ is applied on top and bottom gate electrodes, two channels on top and bottom sides of a-IGZO layer are formed together resulting in steeper SS and higher $I_{ON}$. Furthermore the gate electrodes in the DG structure confine the channel area more effectively. The $V_{TH}$ difference between linear and saturation regime is smaller and the $\mu_{EFF}$ in saturation regime is increased.

### 3.3. Bias-Temperature Stress of DG TFTs

Figure 6 shows the evolution of the DG a-IGZO TFT transfer characteristics under positive BTS (PBTS) and negative BTS (NBTS). The parallel positive shift of I-V curves is observed under PBTS. During NBTS, only a very small shift is observed. From the $V_{TH}$ extracted from Figure 6, the $V_{TH}$ shift ($\Delta V_{TH}$) as a function of bias-temperature stress time is shown in Figure 7. The $\Delta V_{TH}$ is defined by the difference between the $V_{TH}$ after each stress time and initial $V_{TH}$. It should be noticed that all the BTS induced electrical instability can be fully recover after a thermal annealing step (1 hour, 350 C). Each series of BTS experiment is performed on the same TFT and to ensure consistent initial TFT properties, the thermal annealing is applied before each new BTS experiment is conducted.

The $V_{TH}$ shifts of TFTs under PBTS can be explained by charge trapping mechanism, similar to that observed in in amorphous

**Table 1 Extracted device parameters for DG and BG coplanar homojunction a-IGZO TFTs.**

| | BG Bias | | DG Bias | |
|---|---|---|---|---|
| | Lin. | Sat. | Lin. | Sat. |
| $I_{ON}$ [μA] ($V_{GS}$=10V) | 1.3 | 47.0 | 2.0 | 110.0 |
| $I_{OFF}$ [A] | <1×10$^{-13}$ | | <1×10$^{-13}$ | |
| $V_{TH}$ [V] | 0.54 | 0.13 | 0.55 | 0.37 |
| SS [mV] | 153 | 153 | 100 | 99 |
| $\mu_{EFF}$ [$cm^2/V{\cdot}s$] | 12.82 | 9.11 | 13.08 | 15.07 |
| Hysteresis [V] | 0 | | 0 | |
| $C_G$ [nF/$cm^2$] | $C_{BG}$=17.7 | | $C_{DG}$=27.2 | |

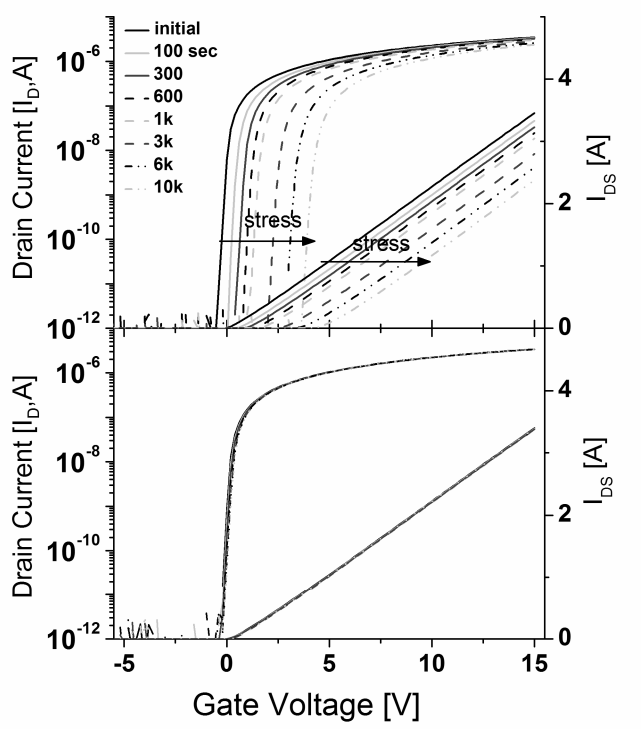


**Figure 6. The evolution of transfer characteristics for (top) positive BTS, $V_{ST}$ = +15V (bottom) negative BTS $V_{ST}$ = -15V. $V_{ST}$ is applied on both top and bottom gate electrodes. The stress temperature is fixed at 80 °C.**

silicon TFTs. The trapping of the negative charges at top and bottom channel / insulator interfaces or/and into the gate insulator near these interfaces will be responsible for observed threshold voltage shift during PBTS. In case of negative BTS the positive charges, holes, should be considered. From the negligibly small $\Delta V_{TH}$ during NBTS, we can conclude that the number of holes in a-IGZO under experimental stress voltage ($V_{ST}$ = -15V) is rather small or the stress voltage is not large enough for holes to overcome a high trapping potential energy barrier. The observed trend (positive shift during PBTS and very small shift during NBTS) is consistent with the previous results obtained for a-IGZO TFT with a-$SiO_x$ as a gate insulator. [10]

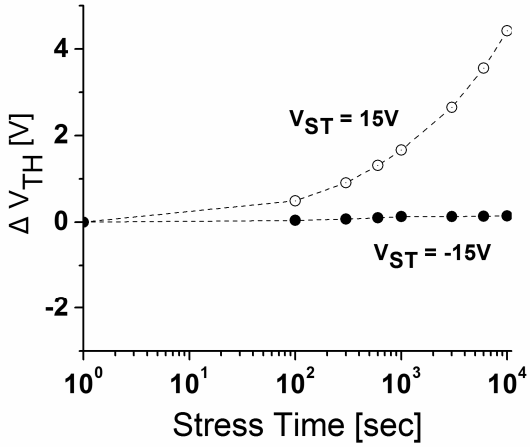


**Figure 7. The variation of $\Delta V_{TH}$ during BTS of the DG TFT; negative BTS (solid) and positive BTS (open).**

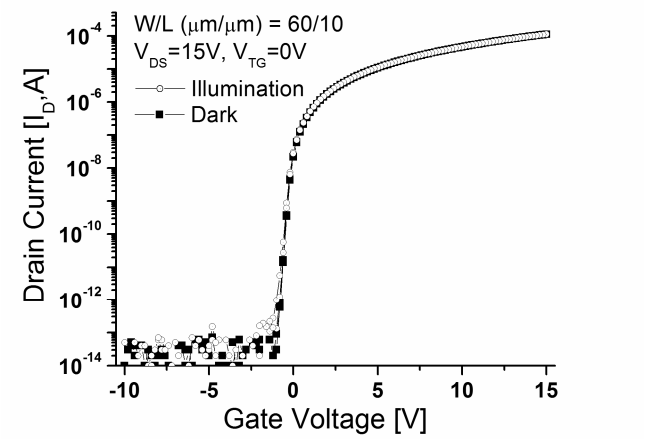


**Figure 8. Transfer characteristic of the DG coplanar homojunction a-IGZO TFT in the dark and under top illumination.**

### 3.4. DG TFT under broadband illumination

We have shown in [9] that the illumination with $\lambda > \lambda_{TH}$ generates the electron-hole pairs (EHP) that will affect the a-IGZO TFT electrical characteristics; the $\lambda_{TH}$ is the threshold wavelength which is closely related to the a-IGZO optical band-gap. No major changes in TFT electrical characteristics occur in the wavelength range, 600 nm (2.07 eV) > λ > 420 nm (2.95 eV). A significant changes on $I_{OFF}$, SS and $V_{TH}$ take place only for λ < 420 nm. For this initial study it was concluded that the a-IGZO TFT will require the light shield when is used in flat panel displays (AM-LCDs or AM-OLEDs) as switching or driving thin-film transistor. One possible approach to realize the TFT light shield is to use the top gate as light shield in DG TFT configuration. Such TFT structure will allow achieving both a high device electrical performance and stable operation under illumination.

To test this idea, we investigated the DG TFT characteristics under light illumination. Figure 8 shows the transfer characteristic of the DG a-IGZO TFT in the dark and under illumination from the top. Both I-V curves are identical. From this result it is clear that in DG TFT structure, the top gate electrode is very effective light shield and should provide stable device operation during front illumination.

## 4. Conclusions

We investigated the electrical characteristics of dual-gate a-IGZO coplanar homojunction TFT with a-SiOx gate insulator. When a gate voltage is applied on top and bottom gate simultaneously, the DG a-IGZO TFT shows desirable electrical performance ($\mu_{EFF}$ = 15.07 $cm^2/V{\cdot}s$, $V_{TH}$ = 0.37 V, SS = 99 mV/dec, $I_{OFF} \sim 10^{-13}$A and on-off ratio over $10^9$) required for next generation flat panel displays. Furthermore $\Delta V_{TH}$ dependence on stress voltage and time was investigated. Under PBTS ($V_{ST}$ = +15V), the $V_{TH}$ of DG TFTs shifts about +4.5V after 10,000 seconds at 80 °C. On the other hand, there is no noticeable $V_{TH}$ shift under NBTS. These BTS results are consistent with the carrier trapping (electrons during PBTS and holes during NBTS) mechanism at the a-IGZO / gate insulator interfaces or within gate insulator itself near these interfaces. Finally, we demonstrated experimentally that the DG TFT is suitable device structure to be used when illumination is present during operation of the flat panel displays.

## 5. Acknowledgements

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